IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR U.S. LETTERS PATENT

Title:

**ACTIVE PIXEL SENSOR WITH A DIAGONAL
ACTIVE AREA**

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FIELD OF THE INVENTION

The invention relates generally to improved semiconductor imaging devices and in particular to a silicon imaging device which can be fabricated using a standard CMOS process. Particularly, the invention relates to CMOS imager

10 having orthogonal row and column lines and a plurality of pixel sensors each having a diagonal active area. The invention further relates to a CMOS imager having two adjacent pixels in the same row of a pixel array connected to a shared column line.

15 ## DESCRIPTION OF THE RELATED ART

There are a number of different types of semiconductor-based imagers, including charge coupled devices (CCDs), photodiode arrays, charge injection devices and hybrid focal plane arrays. CCDs are often employed for image acquisition and enjoy a number of advantages which makes it the

20 incumbent technology, particularly for small size imaging applications. CCDs are also capable of large formats with small pixel size and they employ low noise charge domain processing techniques. However, CCD imagers also suffer from a number of disadvantages. For example, they are susceptible to radiation damage, they exhibit destructive read out over time, they require good light shielding to

25 avoid image smear and they have a high power dissipation for large arrays. Additionally, while offering high performance, CCD arrays are difficult to integrate with CMOS processing in part due to a different processing technology and to their high capacitances, complicating the integration of on-chip drive and

signal processing electronics with the CCD array. While there has been some attempts to integrate on-chip signal processing with the CCD array, these attempts have not been entirely successful. CCDs also must transfer an image by line charge transfers from pixel to pixel, requiring that the entire array be read

5   out into a memory before individual pixels or groups of pixels can be accessed and processed. This takes time. CCDs may also suffer from incomplete charge transfer from pixel to pixel during charge transfer which also results in image smear.

Because of the inherent limitations in CCD technology, there is an

10   interest in CMOS imagers for possible use as low cost imaging devices. A fully compatible CMOS sensor technology enabling a higher level of integration of an image array with associated processing circuits would be beneficial to many digital applications such as, for example, in cameras, scanners, machine vision systems, vehicle navigation systems, video telephones, computer input devices,

15   surveillance systems, auto focus systems, star trackers, motion detection systems, image stabilization systems and data compression systems for high-definition television.

The advantages of CMOS imagers over CCD imagers are that CMOS imagers have a low voltage operation and low power consumption; CMOS

20   imagers are compatible with integrated on-chip electronics (control logic and timing, image processing, and signal conditioning such as A/D conversion); CMOS imagers allow random access to the image data; and CMOS imagers have lower fabrication costs as compared with the conventional CCD since standard CMOS processing techniques can be used. Additionally, low power

25   consumption is achieved for CMOS imagers because only one row of pixels at a time needs to be active during the readout and there is no charge transfer (and associated switching) from pixel to pixel during image acquisition. On-chip

integration of electronics is particularly advantageous because of the potential to perform many signal conditioning functions in the digital domain (versus analog signal processing) as well as to achieve a reduction in system size and cost.

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A CMOS imager circuit includes a focal plane array of pixel cells, each one of the cells including either a photogate, photoconductor or a photodiode overlying a substrate for accumulating photo-generated charge in the underlying portion of the substrate. A readout circuit is connected to each pixel cell and includes at least an output field effect transistor formed in the substrate and a charge transfer section formed on the substrate adjacent the photogate,

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photoconductor or photodiode having a sensing node, typically a floating diffusion node, connected to the gate of an output transistor. The imager may include at least one electronic device such as a transistor for transferring charge from the underlying portion of the substrate to the floating diffusion node and one device, also typically a transistor, for resetting the node to a predetermined

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charge level prior to charge transference.

In a CMOS imager, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) transfer of charge to the floating diffusion node accompanied by charge amplification; (4) resetting the floating diffusion node to a known state

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before the transfer of charge to it; (5) selection of a pixel for readout; and (6) output and amplification of a signal representing pixel charge. Photo charge may be amplified when it moves from the initial charge accumulation region to the floating diffusion node. The charge at the floating diffusion node is typically converted to a pixel output voltage by a source follower output transistor. The

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photosensitive element of a CMOS imager pixel is typically either a depleted p-n junction photodiode or a field induced depletion region beneath a photogate.

For photodiodes, image lag can be eliminated by completely depleting the photodiode upon readout.

CMOS imagers of the type discussed above are generally known as discussed, for example, in Nixon et al., "256 x 256 CMOS Active Pixel Sensor

5   Camera-on-a-Chip," IEEE Journal of Solid-State Circuits, Vol. 31(12) pp. 2046-2050, 1996; Mendis et al, "CMOS Active Pixel Image Sensors," IEEE Transactions on Electron Devices, Vol. 41(3) pp. 452-453, 1994 as well as U.S. Patent No. 5,708,263 and U.S. Patent No. 5,471,515, which are herein incorporated by reference.

10   To provide context for the invention, an exemplary CMOS imaging circuit is described below with reference to FIG. 1. The circuit described below, for example, includes a photogate for accumulating photo-generated charge in an underlying portion of the substrate. It should be understood that the CMOS imager may include a photodiode or other image to charge converting device, in

15   lieu of a photogate, as the initial accumulator for photo-generated charge.

Reference is now made to FIG. 1 which shows a simplified circuit for a pixel of an exemplary CMOS imager using a photogate and having a pixel photodetector circuit 14 and a readout circuit 60. It should be understood that while FIG. 1 shows the circuitry for operation of a single pixel, that in practical

20   use there will be an MxN array of pixels arranged in rows and columns with the pixels of the array accessed using row and column select circuitry, as described in more detail below.

The photodetector circuit 14 is shown in part as a cross-sectional view of a semiconductor substrate 16 typically a p-type silicon, having a surface well of

25   p- type material 20. An optional layer 18 of p-type material may be used if desired, but is not required. Substrate 16 may be formed of, for example, Si,

SiGe, Ge, and GaAs. Typically the entire substrate 16 is p-type doped silicon substrate and may contain a surface p-well 20 (with layer 18 omitted), but many other options are possible, such as, for example p on p- substrates, p on p+ substrates, p-wells in n-type substrates or the like. The terms wafer or substrate

5   used in the description includes any semiconductor-based structure having an exposed surface in which to form the circuit structure used in the invention. Wafer and substrate are to be understood as including , silicon-on-insulator (SOI) technology, silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor

10   foundation, and other semiconductor structures. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure or foundation.

An insulating layer 22 such as, for example, silicon dioxide is formed

15   on the upper surface of p-well 20. The p-type layer may be a p-well formed in substrate 16. A photogate 24 thin enough to pass radiant energy or of a material which passes radiant energy is formed on the insulating layer 22. The photogate 24 receives an applied control signal PG which causes the initial accumulation of pixel charges in n+ region 26. The n+ type region 26, adjacent one side of

20   photogate 24, is formed in the upper surface of p-well 20. A transfer gate 28 is formed on insulating layer 22 between n+ type region 26 and a second n+ type region 30 formed in p-well 20. The n+ regions 26 and 30 and transfer gate 28 form a charge transfer transistor 29 which is controlled by a transfer signal TX. The n+ region 30 is typically called a floating diffusion region. It is also a node

25   for passing charge accumulated thereat to the gate of a source follower transistor 36 described below. A reset gate 32 is also formed on insulating layer 22 adjacent and between n+ type region 30 and another n+ region 34 which is also

formed in p-well 20. The reset gate 32 and n+ regions 30 and 34 form a reset transistor 31 which is controlled by a reset signal RST. The n+ type region 34 is coupled to voltage source VDD, e.g., 5 volts. The transfer and reset transistors 29, 31 are n-channel transistors as described in this implementation of a CMOS

5   imager circuit in a p-well. It should be understood that it is possible to implement a CMOS imager in an n-well in which case each of the transistors would be p-channel transistors. It should also be noted that while FIG. 1 shows the use of a transfer gate 28 and associated transistor 29, this structure provides advantages, but is not required.

10   Photodetector circuit 14 also includes two additional n-channel transistors, source follower transistor 36 and row select transistor 38. Transistors 36, 38 are coupled in series, source to drain, with the source of transistor 36 also coupled over lead 40 to voltage source VDD and the drain of transistor 38 coupled to a lead 42. The drain of row select transistor 38 is connected via

15   conductor 42 to the drains of similar row select transistors for other pixels in a given pixel row. A load transistor 39 is also coupled between the drain of transistor 38 and a voltage source VSS, e.g. 0 volts. Transistor 39 is kept on by a signal VLN applied to its gate.

The imager includes a readout circuit 60 which includes a signal

20   sample and hold (S/H) circuit including a S/H n-channel field effect transistor 62 and a signal storage capacitor 64 connected to the source follower transistor 36 through row transistor 38. The other side of the capacitor 64 is connected to a source voltage VSS. The upper side of the capacitor 64 is also connected to the gate of a p-channel output transistor 66. The drain of the output transistor 66 is

25   connected through a column select transistor 68 to a signal sample output node VOUTS and through a load transistor 70 to the voltage supply VDD. A signal called "signal sample and hold" (SHS) briefly turns on the S/H transistor 62

after the charge accumulated beneath the photogate electrode 24 has been transferred to the floating diffusion node 30 and from there to the source follower transistor 36 and through row select transistor 38 to line 42, so that the capacitor 64 stores a voltage representing the amount of charge previously

5   accumulated beneath the photogate electrode 24.

The readout circuit 60 also includes a reset sample and hold (S/H) circuit including a S/H transistor 72 and a signal storage capacitor 74 connected through the S/H transistor 72 and through the row select transistor 38 to the source of the source follower transistor 36. The other side of the capacitor 74 is

10   connected to the source voltage VSS. The upper side of the capacitor 74 is also connected to the gate of a p-channel output transistor 76. The drain of the output transistor 76 is connected through a p-channel column select transistor 78 to a reset sample output node VOUTR and through a load transistor 80 to the supply voltage VDD. A signal called "reset sample and hold" (SHR) briefly

15   turns on the S/H transistor 72 immediately after the reset signal RST has caused reset transistor 31 to turn on and reset the potential of the floating diffusion node 30, so that the capacitor 74 stores the voltage to which the floating diffusion node 30 has been reset.

The readout circuit 60 provides correlated sampling of the potential of the floating diffusion node 30, first of the reset charge applied to node 30 by

20   reset transistor 31 and then of the stored charge from the photogate 24. The two samplings of the diffusion node 30 charges produce respective output voltages VOUTR and VOUTS of the readout circuit 60. These voltages are then subtracted (VOUTS-VOUTR) by subtractor 82 to provide an output signal

25   terminal 81 which is an image signal independent of pixel to pixel variations caused by fabrication variations in the reset voltage transistor 31 which might cause pixel to pixel variations in the output signal.

FIG. 2 illustrates a block diagram for a CMOS imager having a pixel array 200 with each pixel cell being constructed in the manner shown by element 14 of FIG. 1. Pixel array 200 comprises a plurality of pixels arranged in a predetermined number of columns and rows. The pixels of each row in array

5   200 are all turned on at the same time by a row select line, e.g., line 86, and the pixels of each column are selectively output by a column select line, e.g., line 42. A plurality of rows and column lines are provided for the entire array 200. The row lines are selectively activated by the row driver 210 in response to row address decoder 220 and the column select lines are selectively activated by the

10   column driver 260 in response to column address decoder 270. Thus, a row and column address is provided for each pixel. The CMOS imager is operated by the control circuit 250 which controls address decoders 220, 270 for selecting the appropriate row and column lines for pixel readout, and row and column driver circuitry 210, 260 which apply driving voltage to the drive transistors of the

15   selected row and column lines.

FIG. 3 shows a simplified timing diagram for the signals used to transfer charge out of photodetector circuit 14 of the FIG. 1 CMOS imager. The photogate signal PG is nominally set to 5V and pulsed from 5V to 0V during integration. The reset signal RST is nominally set at 2.5V. As can be

20   seen from the figure, the process is begun at time t_0 by briefly pulsing reset voltage RST to 5V. The RST voltage, which is applied to the gate 32 of reset transistor 31, causes transistor 31 to turn on and the floating diffusion node 30 to charge to the VDD voltage present at n+ region 34 (less the voltage drop Vth of transistor 31). This resets the floating diffusion node 30 to a predetermined

25   voltage (VDD-Vth). The charge on floating diffusion node 30 is applied to the gate of the source follower transistor 36 to control the current passing through transistor 38, which has been turned on by a row select (ROW) signal, and load

transistor 39. This current is translated into a voltage on line 42 which is next sampled by providing a SHR signal to the S/H transistor 72 which charges capacitor 74 with the source follower transistor output voltage on line 42 representing the reset charge present at floating diffusion node 30. The PG

5   signal is next pulsed to 0 volts, causing charge to be collected in n+ region 26. A transfer gate voltage TX, similar to the reset pulse RST, is then applied to transfer gate 28 of transistor 29 to cause the charge in n+ region 26 to transfer to floating diffusion node 30. It should be understood that for the case of a photogate, the transfer gate voltage TX may be pulsed or held to a fixed DC

10   potential. For the implementation of a photodiode with a transfer gate, the transfer gate voltage TX must be pulsed. The new output voltage on line 42 generated by source follower transistor 36 current is then sampled onto capacitor 64 by enabling the sample and hold switch 62 by signal SHS. The column select signal is next applied to transistors 68 and 70 and the respective charges stored in

15   capacitors 64 and 74 are subtracted in subtractor 82 to provide a pixel output signal at terminal 81. It should also be noted that CMOS imagers may dispense with the transfer gate 28 and associated transistor 29, or retain these structures while biasing the transfer transistor 29 to an always "on" state.

The operation of the charge collection of the CMOS imager is known in

20   the art and is described in several publications such as Mendis et al., "Progress in CMOS Active Pixel Image Sensors," SPIE Vol. 2172, pp. 19-29 1994; Mendis et al., "CMOS Active Pixel Image Sensors for Highly Integrated Imaging Systems," IEEE Journal of Solid State Circuits, Vol. 32(2), 1997; and Eric R. Fossum, "CMOS Image Sensors: Electronic Camera on a Chip," IEDM Vol. 95

25   pages 17-25 (1995) as well as other publications. These references are incorporated herein by reference.

Prior CMOS imagers had a respective column line attached to every pixel in the row. By having a column line for each pixel in the row, the row select (ROW), reset (RST) and transfer (TX) lines of the prior imagers had to be routed in a manner where such lines are not straight and, in fact, each have

5   substantial perpendicular conductive segments 811, 816, 851 respectively, as shown in FIG. 7. The large number of perpendicular conductor segments makes fabrication of a pixel array complicated and it is difficult to maintain the required spacing for the numerous conductors and their perpendicular segments. Additionally, CMOS imagers having such a considerable number of non-linear

10   contact paths results in increased materials costs and a large pixel size. It would be desirable to shrink pixel size if possible to reduce the size of the conductors in order to increase the size of the photosensitive area "active area" of a pixel.

15   <u>SUMMARY OF THE INVENTION</u>

The present invention provides an imaging device formed as a CMOS integrated circuit using a standard CMOS process fabricated such that two adjacent pixels in a selected row share a single column line. By sharing column lines, the pixel array can be fabricated using fewer conductors which permits the

20   cells to have larger photosensitive areas. Additionally, by having two adjacent pixels sharing a single column line the imager will be more efficiently fabricated since the design of the present invention eliminates half of the usually required metal column line contacts.

The present invention seeks to reduce the number of required

25   conductors having perpendicular segments while providing orthogonal row and column conductors for the pixel array. In one implementation of the invention the shared column lines and straight contact lines are achieved by formulating a

diagonal active area for each pixel. The fabrication of the diagonal active area

allows the row select lines and column select and reset lines to be linear in the

circuit (when viewed from above). The diagonal active area implementation of

the present invention also allows displacement of the metal Vout lines from the

5   VDD contacts so that the Vout lines can be straight.

The above and other advantages and features of the invention will be

more clearly understood from the following detailed description which is

provided in connection with the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages and features of the invention will

become more apparent from the detailed description of the preferred

embodiments of the invention given below with reference to the accompanying

15   drawings in which:

FIG. 1 is a representative circuit of a CMOS imager.

FIG. 2 is a block diagram of a CMOS active pixel sensor chip.

FIG. 3 is a representative timing diagram for the CMOS imager.

FIG. 4 shows a pixel layout showing a 2x3 pixel layout according to

20   the prior art.

FIG. 5 shows a pixel layout showing a 2x3 pixel layout according to

one embodiment of the present invention.

FIG. 6 is a representative layout of a CMOS array according to the

present invention showing two rows of pixels sharing a single column line.

FIG. 7 is a layout illustrating a prior CMOS imager.

FIG. 8 is a layout illustrating a CMOS imager of the present invention having a diagonal active area.

FIG. 9 is an illustration of a computer system having a CMOS imager according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will now be described with reference to the figures. Referring now to FIG. 4. This figure shows a 2x3 pixel layout according to the prior art. Pixels 301, 302 and 303 contact column line 310 and row lines 312, 314 and 316. Pixels 304, 305 and 306 contact column line 311 and row lines 312, 314 and 316.

FIG. 5 illustrates a similar 2x3 pixel layout according to one embodiment of the present invention. As illustrated in the figure, pixels 401, 402, 403, 404, 405 and 406 all connect with column line 410. Pixel 401 connects with even row line 412. Pixel 402 connects with even row line 414. Pixel 403 connects with even row line 416. Pixel 404 connects with odd row line 411. Pixel 405 connects with odd row line 413. Pixel 406 connects with odd row line 415. As can be seen from FIG. 5, all six pixels connects with a single column line 410. Row lines (411, 412, 413, 414, 415, 416) are conventionally formed of doped polysilicon, metals; such as tungsten, titanium, titanium nitride; and refractory metal silicides; such as tungsten silicide, titanium silicide, tantalum silicide or cobalt silicide and mixtures thereof. The column line (410) is formed of a metal layer. By eliminating half of the sensor array metal layer column lines, as shown in FIG. 6, the overall size of the CMOS imager

device can be reduced and/or the size of the photosensitive area can be increased.

FIG. 6 shows a plurality of pixels (501, 502, 503, 504, 505, 506, 507, 508) located in an array 500. It should be understood that the labeled pixels of FIG. 6 generally function similar to the pixels previously described with respect to FIG. 1. Pixels 501, 502, 504 and 505 are connected by a shared column line 515. Pixels 503, 506, 507 and 508, for example, are connected to a second shared column line 517. Although pixels 501, 502, 504 and 505 are addressed using a single column line 515, pixel 501 is addressed by odd row line 522, and pixel 502 is addressed by even row line 524, pixel 504 is addressed by odd row line 526 and pixel 505 is addressed by even row line 528. Thus, even though adjacent row pixels, e.g., 501, 502 share a single column line, e.g., 515 their addresses are not identical.

When the active area is fabricated to be generally linear, the prior art imagers needed to fabricate the output, VDD, reset, and row select lines in the device in a non-linear configuration with conductors having perpendicular segments, as shown in FIG. 7. As can be seen from the figure, the pixel cell includes an active area 802 having a general L-shape. Every pixel cell includes a single column line 805 where the voltage of the pixel cell is output to the readout circuit via metal connection 840. As can be seen from the figure, transfer line 850 and row line 810 each have a perpendicular segments, 851 and 811 respectively, in order to effectively connect and operate the pixel cell. The pixel cell also has a reset line 830 which has two perpendicular segments 816. The cell is connected to VDD by line 820.

FIG. 8 is a layout in accordance with the invention illustrating a CMOS imager having a diagonal active area component 643, 644 and linear and

orthogonal row 610, 612 and column 605 lines and linear reset lines 614, 616 which parallel the row lines. By fabricating an active area 601, 602 having a diagonal component 643, 644, the present invention allows the fabrication of straight reset, row select, VDD and Vout column lines. The diagonal fabrication

5   of the active area also facilitates the connection of two cells to a single shared column line, which reduces the number of column contacts over the prior arrays.

As illustrated in FIG. 8, a straight column line 605 connects two CMOS imager cells 603, 604 at connection point 640. The first cell 603 has an active area (sensor area) 602 which includes a diagonal component 643. The

10   row select transistor of the first cell 603 is addressed by even row select line 610. The cell reset 603 is activated by reset line 614. The gate of the source follower transistor is connected by line 630. The cell 603 is connected to VDD by contact 620.

The second cell 604 has an active area (sensor area) 601 which includes a diagonal component 644. The row select transistor of the second cell

15   604 is addressed by odd row select line 612. The reset transistor of cell 604 is activated by reset line 616. The gate of the source follower transistor is connected to logic by line 632. The cell 604 is connected to VDD by contact 622. As illustrated in the figure, the row select lines 610, 612 and the reset lines

20   614, 616 are patterned to be straight. Additionally, the column line 605 is also straight and the two cells 603, 604 are connected to the single column line 605. The active areas 601, 602 when top viewed as in FIG. 8 for a general S-shaped configuration.

The use of a diagonal active area for the pixel allows better contact

25   between the pixel and the associated circuit logic because the chance of forming improper contacts during fabrication is reduced with a straight line.

Additionally, the diagonal active area displaces the column line contact from the VDD contacts so that the metal lines can be straight. The diagonal active area also facilitates the sharing of a single column line by adjacent row pixels.

5   A typical processor based system which includes a CMOS imager device according to the present invention is illustrated generally at 700 in Fig. 9. A processor based system is exemplary of a system having digital circuits which could include CMOS imager devices. Without being limiting, such a system could include a computer system, camera system, scanner, machine vision system, vehicle navigation system, video telephone system, surveillance system, auto

10   focus system, star tracker system, motion detection system, image stabilization system and data compression system for high-definition television, all of which can utilize the present invention.

     A processor system, such as a computer system, for example generally comprises a central processing unit (CPU) 744 e.g., a microprocessor, that

15   communicates with an input/output (I/O) device 446 over a bus 752. The CMOS imager 742 also communicates with the system over bus 752. The CMOS imager 742 may be combined with a processor, such as a CPU 744, a digital signal processor or microprocessor, in a single integrated circuit.

     The computer system 700 also includes random access memory

20   (RAM) 748, and, in the case of a computer system may include peripheral devices such as a floppy disk drive 754 and a compact disk (CD) ROM drive 756 which also communicate with CPU 744 over the bus 752. CMOS imager 742 is preferably constructed as an integrated circuit which includes an integrated circuit as previously described with respect to FIGS. 5-6 and 8.

25   It should again be noted that although the invention has been described with specific reference to specific CMOS circuits having a single

column line and even and odd row lines, the invention has broader applicability and may be used in any imaging apparatus. For example, the invention is not limited to the diagonal active area implementation. Any physical arrangement of adjacent pixels which allows adjacent multiple cells to contact a single column

5   line is within the scope of the present invention. Similarly, the process described above is but one method of many that could be used. Accordingly, the above description and accompanying drawings are only illustrative of preferred embodiments which can achieve the features and advantages of the present invention. It is not intended that the invention be limited to the embodiments

10   shown and described in detail herein. The invention is only limited by the scope of the following claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is: